EE 435 Lecture 41

Phased Locked Loops and VCOs Over Sampled Data Converters

Final Exam:

Scheduled on Final Exam Schedule:

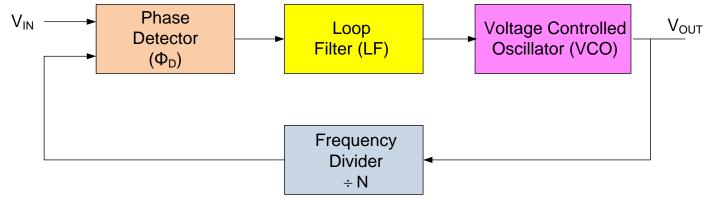
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Wednesday May 5 9:45 a.m.
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Revised Final Exam:

- Take-home format open book and open notes
- Will be posted on course WEB site by late Friday April 30
- Due at 5:00 p.m. on Wednesday May 5 : Upload as pdf file into Canvas

If anyone has any constraints of any form such as internet access or other factors that makes it difficult to work with this revised format, please contact Professor Geiger by 5:00 p.m. on Wednesday April 28

Basic PLL Architecture

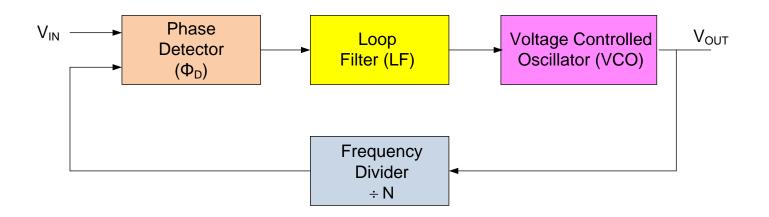


Applications include:

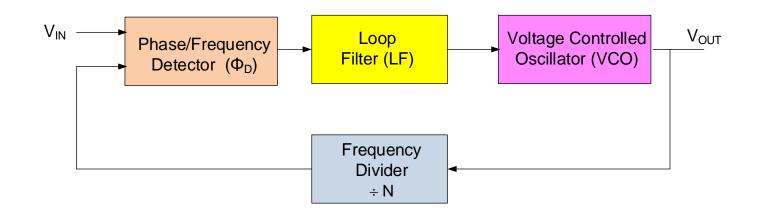
Frequency Demodulation Frequency Synthesis Clock Synchronization Noise filtering (extreme) Tracking and calibrated filters

- One of the most widely used analog blocks
- Many SoC systems include multiple PLLs
- Closely related to Delay Locked Loop (DLL)

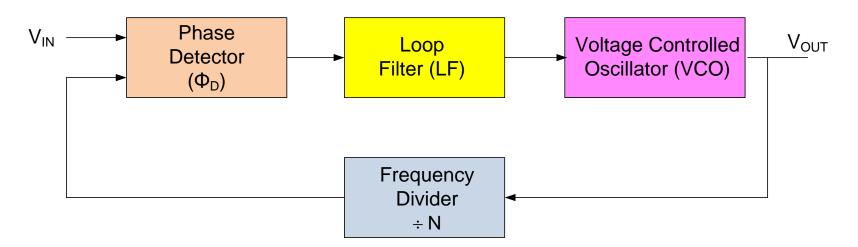
Basic PLL Architecture



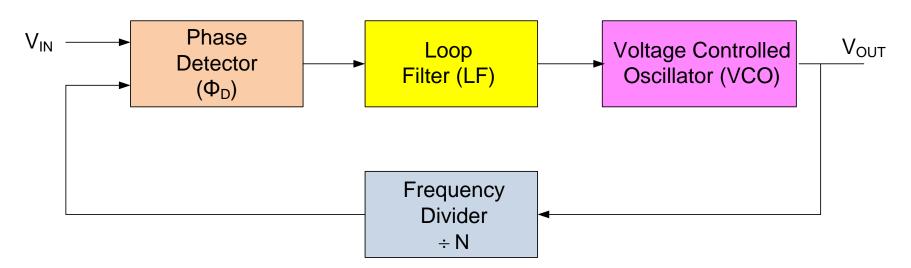
Often actually use phase/frequency detector but still termed PLL



Basis PLL Architecture



Applications by subcategory: Clock and Data Recovery Recovering signals when SNR <<<1 Timing generators in digital systems

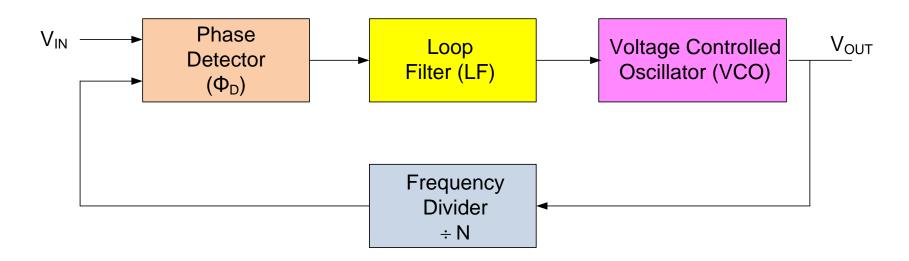


 $V_{IN}=V_{M}sin(\omega_{IN}t+\varphi_{IN})$

Desired output when locked:

 $V_{OUT} = V_X sin(N\omega_{IN}t + \phi_{OUT})$

- Relationship between V_{M} and V_{X} is of little concern
- Frequency relationship is critical
- ϕ_{OUT} is often critical too
- Waveshape of V_{IN} and V_{OUT} is often of little concern May be highly distorted or even square waves



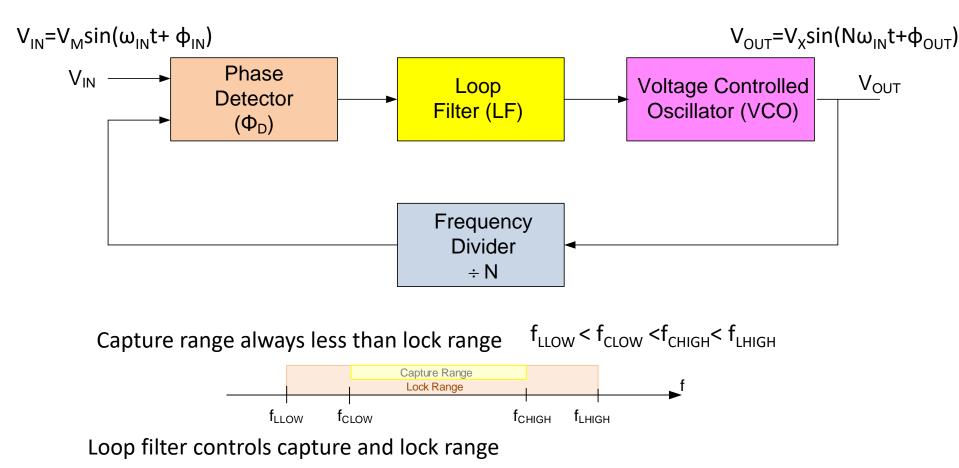
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Desired output when locked:

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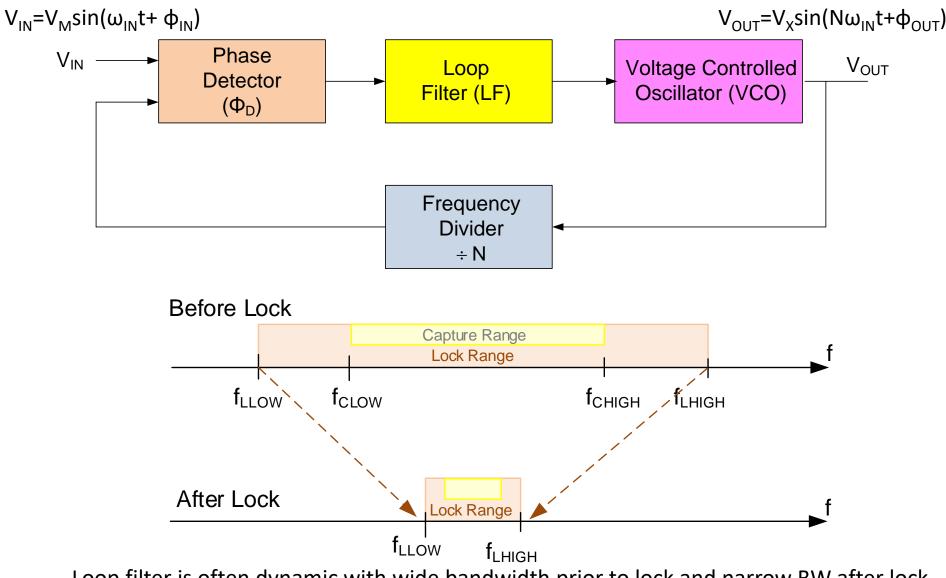
Some Terminology of PLLs

Locked / UnlockedLocked when V_{OUT} assumes desired valueLock RangeLocked when V_{OUT} assumes desired valueCapture Range $f_{LLOW} < f_{IN} < f_{LHIGH}$ Free-running frequency $f_{CLOW} < f_{IN} < f_{CHIGH}$ Harmonic/Subharmonic LockLocked when VOUT assumes desired value



Jitter in VCO output strongly dependent upon lock range (large lock range results in high jitter, low lock range in low jitter)

Loop filter is often dynamic with wide bandwidth prior to lock and narrow BW after lock



Loop filter is often dynamic with wide bandwidth prior to lock and narrow BW after lock

Conceptual Operation of PLL

Consider a signal defined for $-\infty < t < \infty$ expressed as

 $V(t) = V_M sin(\phi(t))$

If the signal is sinusoidal with frequency ω , the argument ϕ can be expressed as

 $\phi(t)=\omega t+\theta$

where ϕ is defined to be the phase of the signal and θ is the phase offset on the time axis from the time reference t=0

Taking the time derivative of $\phi(t)$, we obtain

$$\frac{d\phi}{dt} = \omega$$

Taking the Laplace Transform, we have

$$\phi_{\rm S} = \frac{\omega}{\rm S}$$

Is the second statement "If the signal is sinusoidal" redundant ?

Is the second statement "If the signal is sinusoidal" redundant?

Consider a signal defined for $-\infty < t < \infty$ expressed as

 $V(t) = V_M sin(\phi)$

If the signal is sinusoidal with frequency ω , the argument ϕ can be expressed as

 $\phi = \omega t + \theta$

Consider any signal f(t) defined for all time (not necessarily periodic but could be)

Define $\phi(t)$ by the expression $\phi(t) = \sin^{-1}\left(\frac{f(t)}{V_M}\right)$

It follows that
$$V(t) = V_{M} \sin(\phi(t)) = V_{M} \sin\left(\sin^{-1}\left(\frac{f(t)}{V_{M}}\right)\right) = f(t)$$

Thus, the first statement gives NO information about the signal V(t)

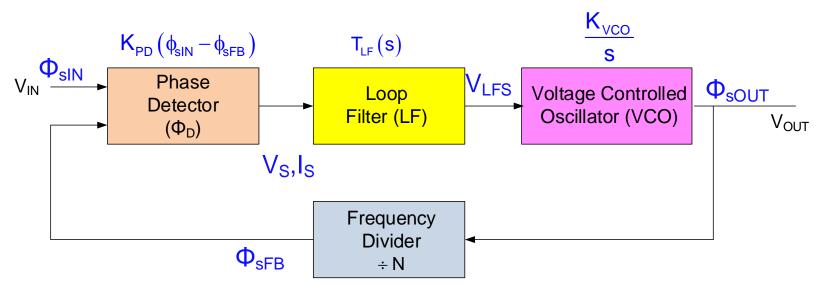
Consider a VCO where the output is sinusoidal

Assume the output of interest is the phase ϕ

$$V_{LF} \qquad Voltage Controlled \\ Oscillator (VCO) \qquad \Phi \quad V_{OUT} \\ \varphi(t) = \omega t + \theta \\ V_{OUT} = V_m \sin(\omega t + \theta) \\ \omega = V_{LF} \bullet K_{VCO} \\ \frac{d\phi}{dt} = \omega = V_{LF} K_{VCO} \\ Taking Laplace Transform: S\phi_S = V_{LFS} K_{VCO} \qquad \longrightarrow \quad \phi_S = V_{LFS} \frac{K_{VCO}}{S} \\ V_{LFS} \qquad K_{VCO} \qquad \Phi_S = V_{LFS} \frac{K_{VCO}}{S} \\ V_{CO} \qquad V_{OUT} \\ V_{CO} \qquad V_{CO} \\ V_{CO} \\ V_{CO} \\ V_{CO} \\ V_{CO} \\ V_{CO} \\ V_{C$$

Conceptual Operation of PLL

- When locked, PLL can be modeled as a linear system
- Small-signal s-domain analysis when PLL is locked



Note: Dimensions of variables in loop are not the same

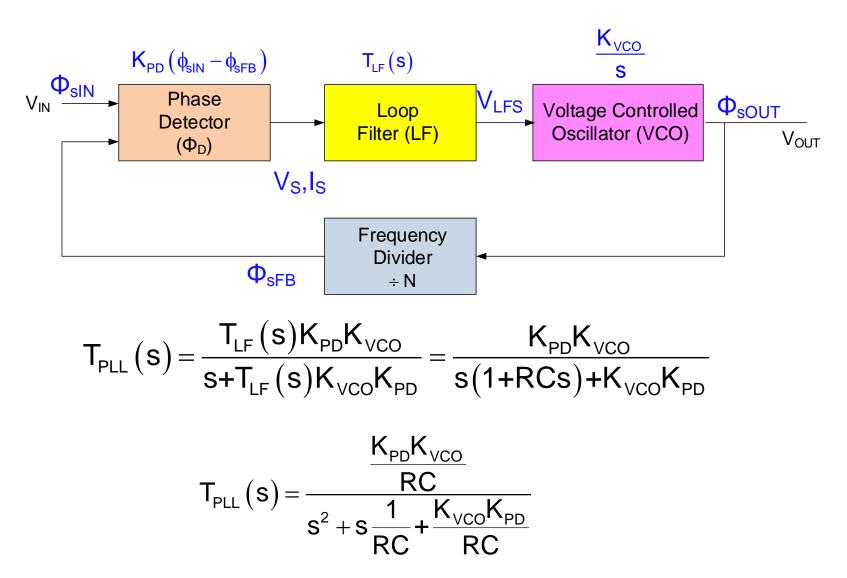
$$V = K_{PD} \left(\phi_{sIN} - \phi_{sFB} \right)$$
$$V_{LF} = T_{LF} \left(s \right) V$$
$$\phi_{sOUT} = V_{LF} \frac{K_{VCO}}{s}$$
$$\phi_{sFB} = \frac{\phi_{sOUT}}{N}$$

Solving, we obtain

$$T_{PLL}(s) = \frac{\phi_{sOUT}}{\phi_{sIN}} = \frac{T_{LF}(s)K_{PD}K_{VCO}}{s+T_{LF}(s)\frac{K_{VCO}K_{PD}}{N}}$$

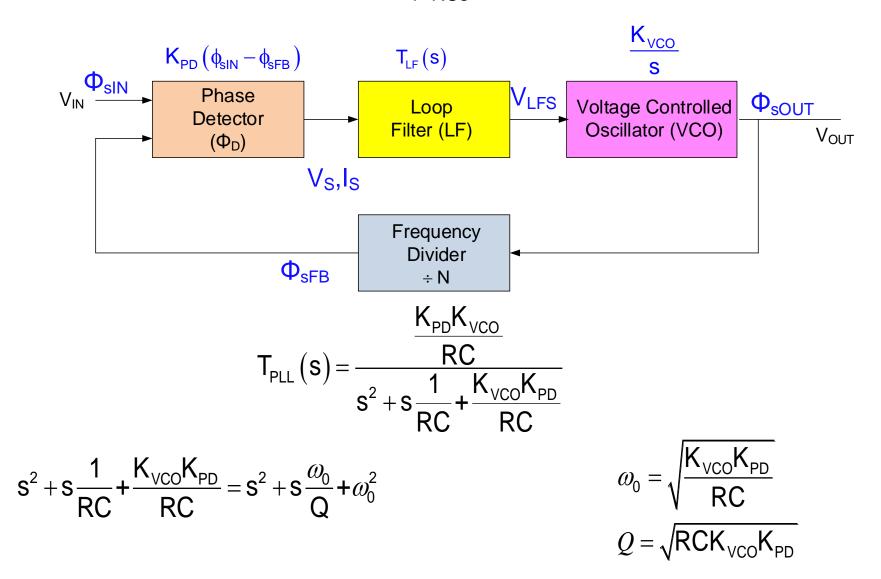
Often the LF is low order

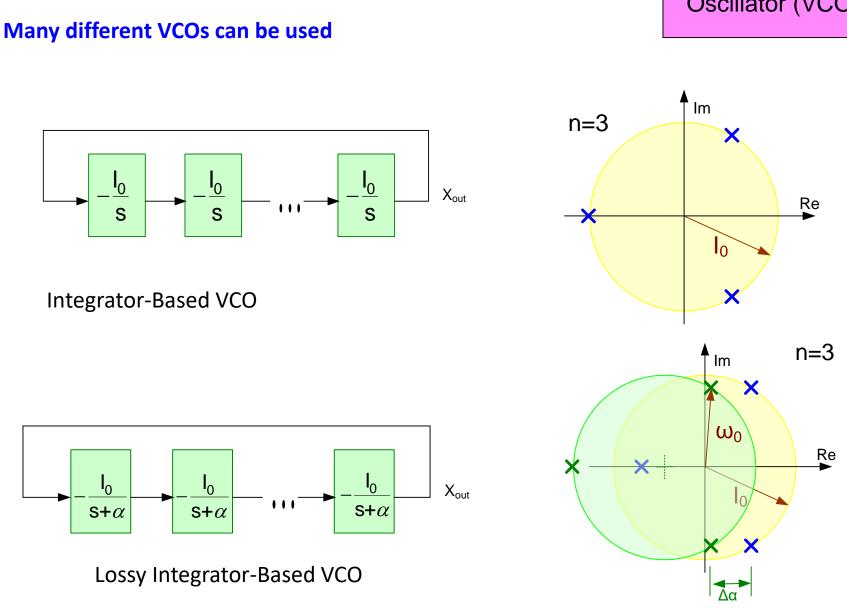
Example: Assume N=1 and $T_{LF}(s) = \frac{1}{1+RCs}$



Often the LF is low order

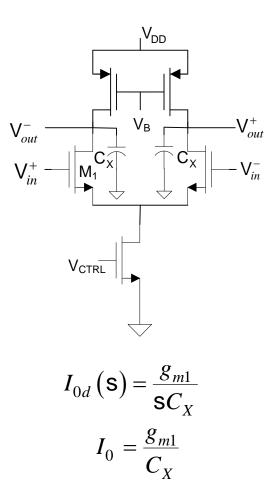
Example: Assume N=1 and $T_{LF}(s) = \frac{1}{1+RCs}$





Voltage Controlled Oscillators

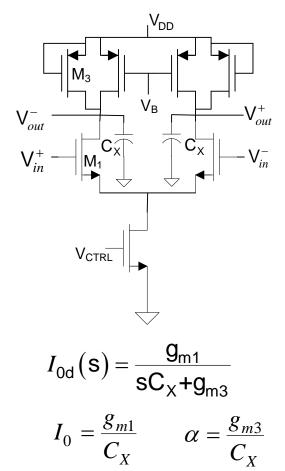
Voltage Controlled Oscillator (VCO)



Voltage Controlled Oscillators

Integrator for: Integrator-based VCO

Voltage Controlled Oscillator (VCO)

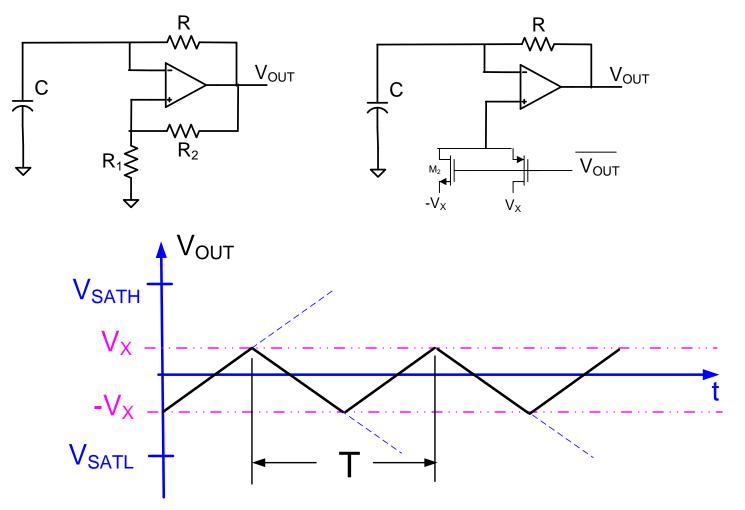


Integrator for: Lossy Integrator-based VCO

Voltage Controlled Oscillators

Voltage Controlled Oscillator (VCO)

Relaxation Oscillator Derived VCO

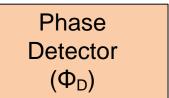


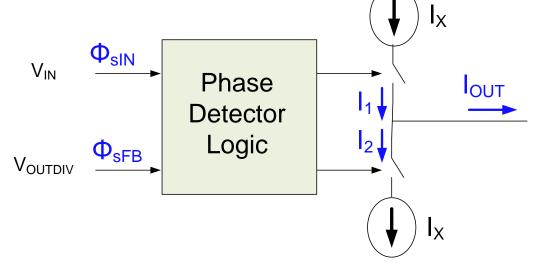
Can have either triangle wave or square wave ouputs

Phase Detectors

Many different Phase Detectors can be used

Some Popular Phase Detector Circuits Analog Multiplier Exclusive OR Gate Sample and Hold Charge Pump



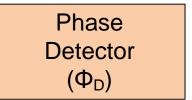


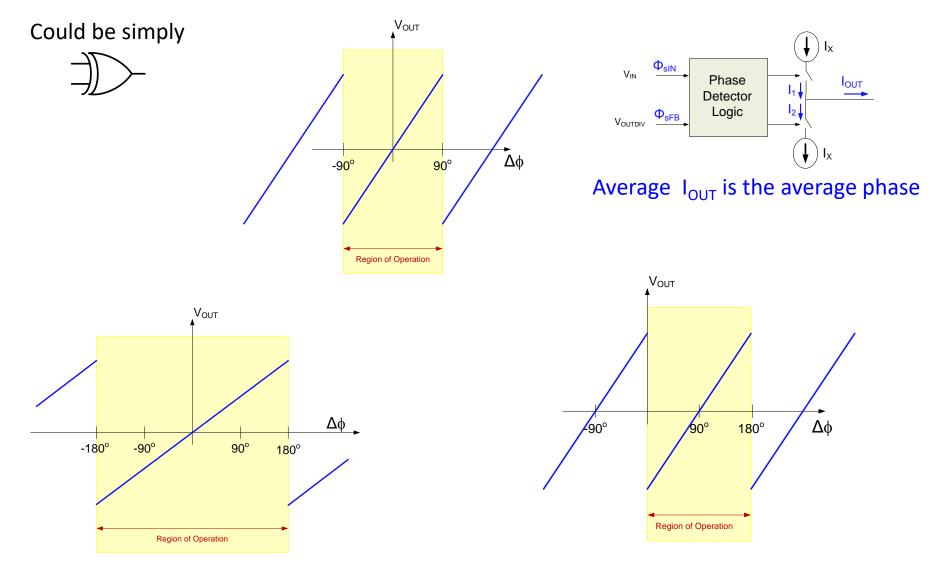
Charge-pump based Phase Detector

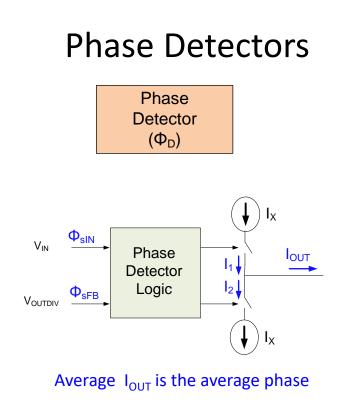
Average I_{OUT} is the average phase

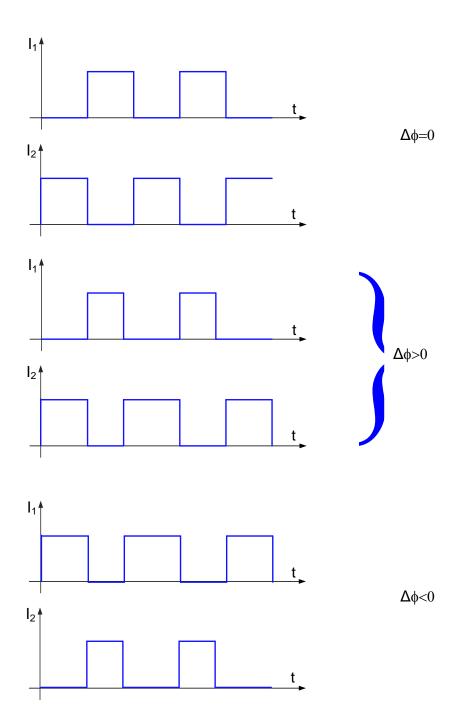
Phase Detectors

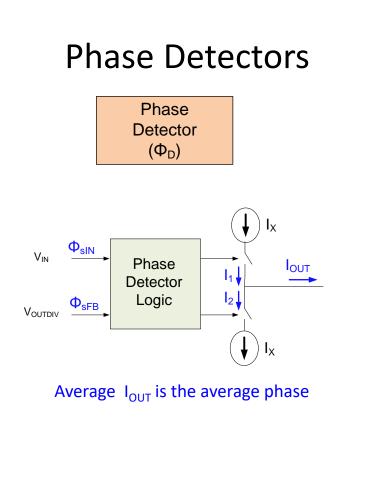
Many different Phase Detectors can be used

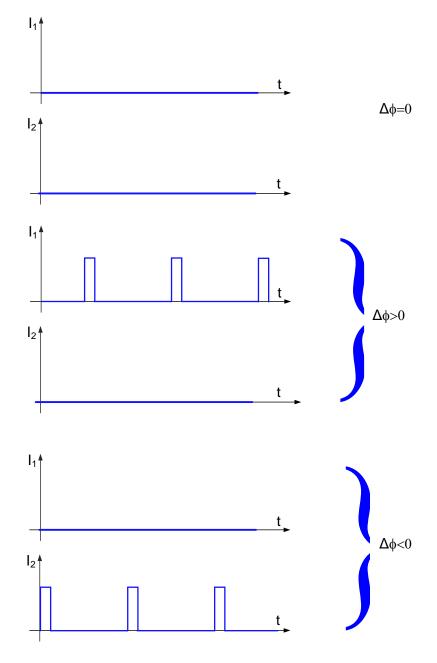










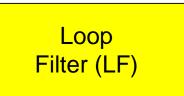


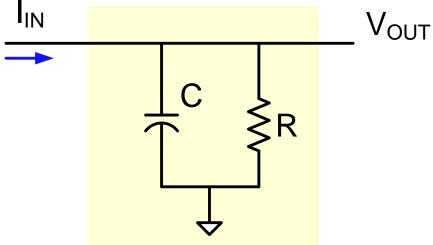
Vulnerable to dead zone problem

Loop Filters

Many different Phase Detectors can be used Often the loop filter is first or second order Usually the loop filter circuit is very simple

$T_{LF}(s)$



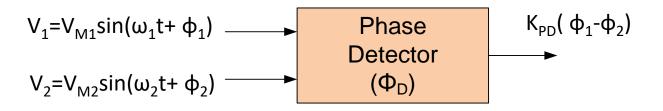




 $\frac{V_{OUT}}{I_{INAVG}} = T_{LF}(s) = \frac{R}{1 + RCs}$

Basic first-order LF with average current difference as input

What is the phase of a signal?



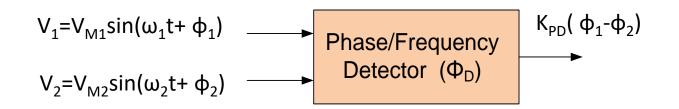
Assume $\omega_1 = \omega_2 = \omega$

If V₁ can be expressed as $V_1 = V_{M1} \sin(\omega t + \phi_1)$ the phase is ϕ_1

But what is the phase if ω is time varying? Or what is the "phase" if this functional form does not really characterize V(t)? Or what if $\omega_1 \neq \omega_2$?

What does a phase detector do if the two inputs are not at the same frequency?

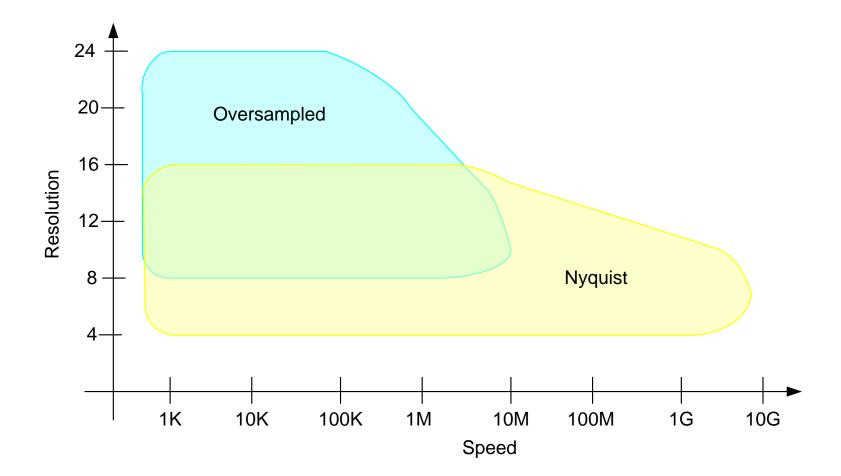
What is the phase of a signal?



Most Phase Detectors are actually Phase/Frequency Detectors

- Large output when frequency difference exists
- Also provides output when phase difference exists after frequencies are matched

Data Converter Type Chart

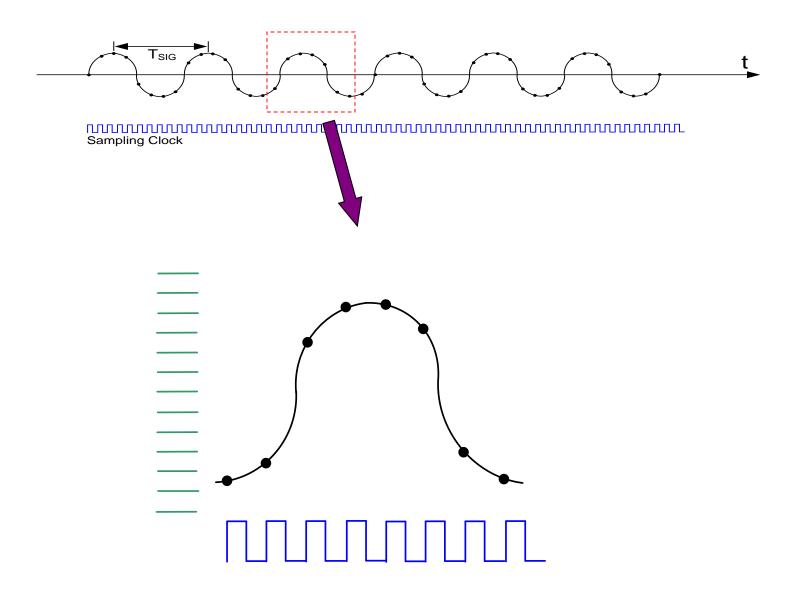


Over-Sampled Data Converters

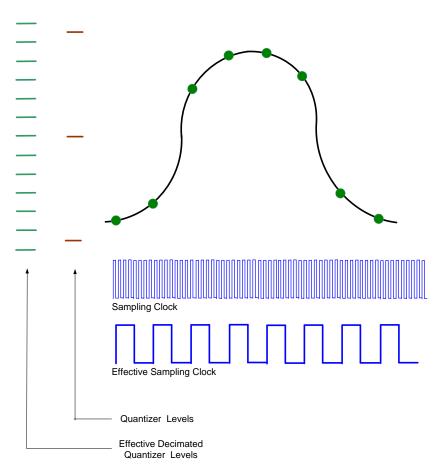
General Classes

- Single-bit
- Multi-bit
- First-order
- Higher-order
- Continuous-time

Nyquist Rate



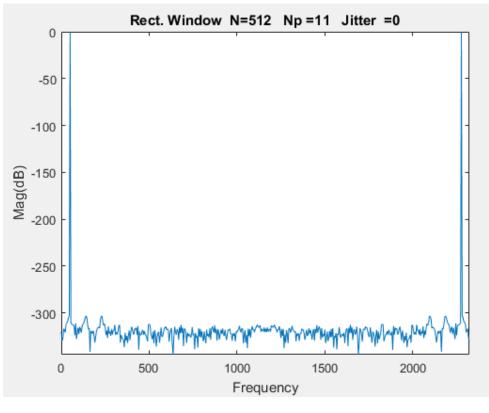
Over-Sampled



Over-sampling ratios of 128:1 or 64:1 are common Dramatic reduction in quantization noise effects Limited to relatively low frequencies

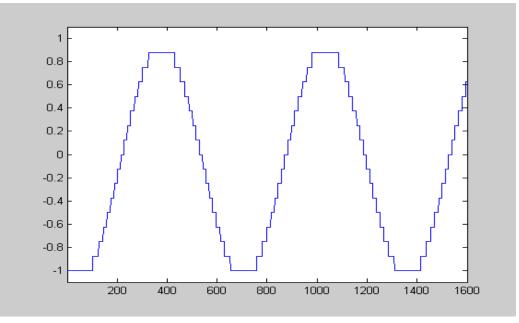
Recall:

f_{SIG}=50Hz f_{NYQ}=100Hz f_{SAMP}=2.3KHz Oversampled: 23:1



MatLab Results

Recall: Quantization Effects



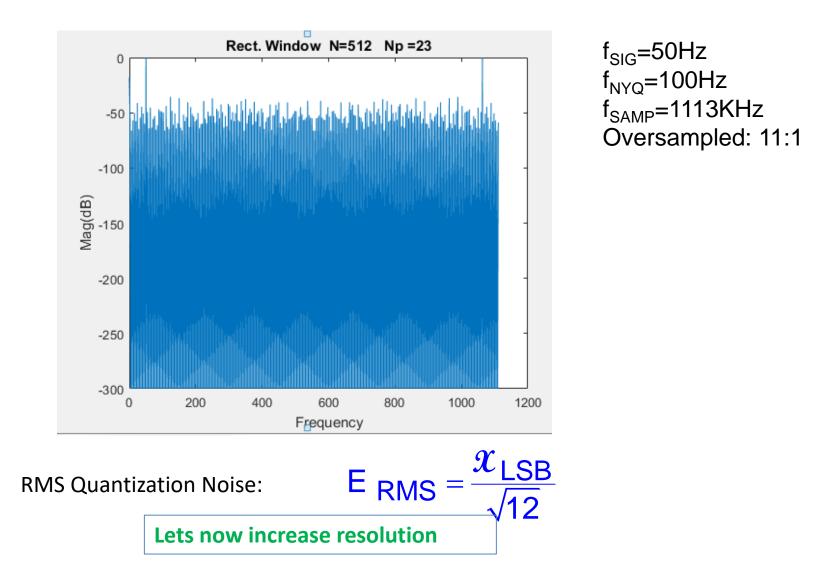
Simulation environment:

N_P=23 f_{SIG}=50Hz



Quantization Effects

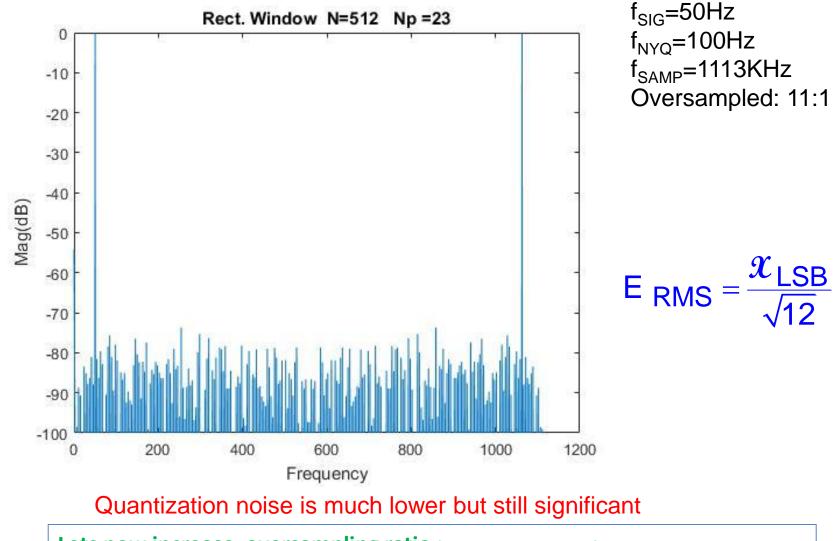
Res = 4 bits



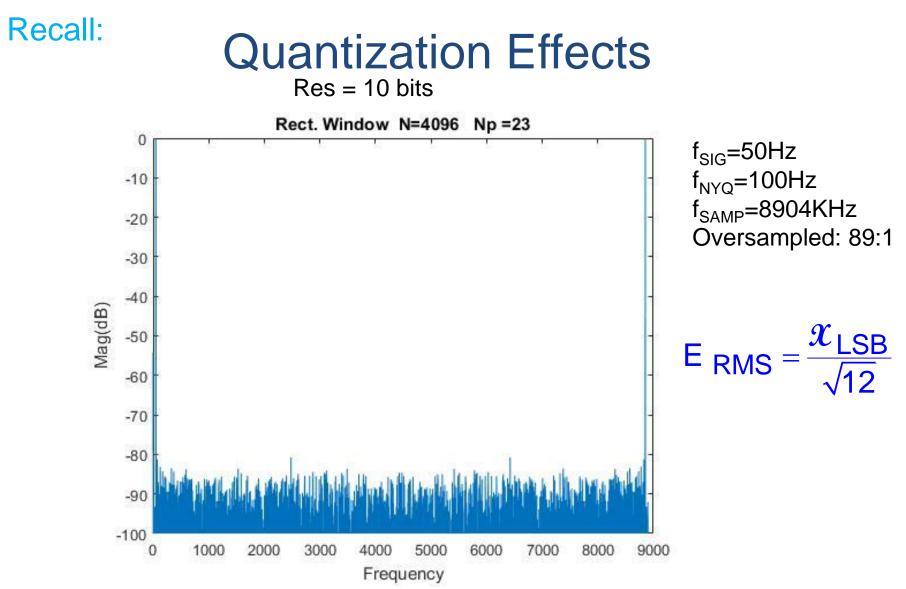
Quantization Effects

Res = 10 bits

Recall:



Lets now increase oversampling ratio (i.e. number of samples)



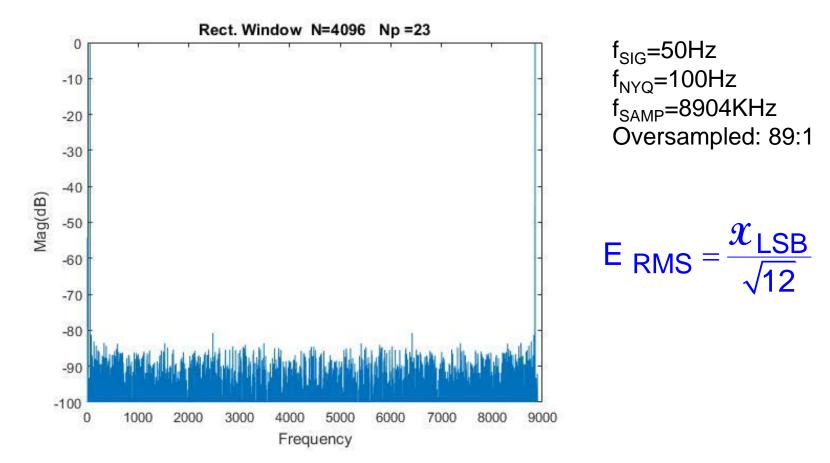
Compared to the previous slide, it appears that the quantization noise has gone down

But has it ? Magnitude of quantization DFT terms decreased but E_{RMS} unchanged

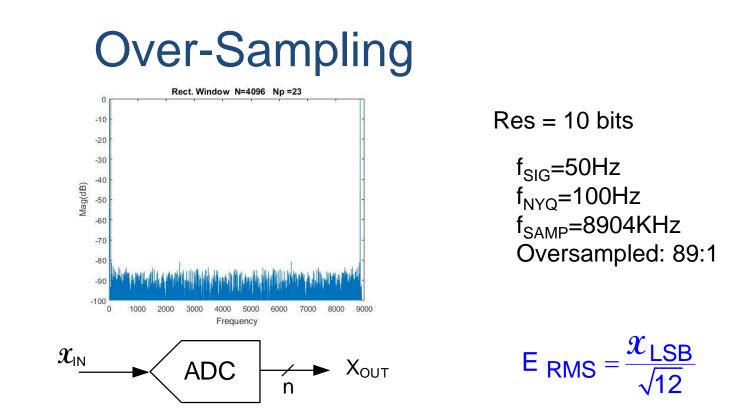


Quantization Effects

Res = 10 bits



Can any additional useful information about the input be obtained since we have many more samples than are needed?

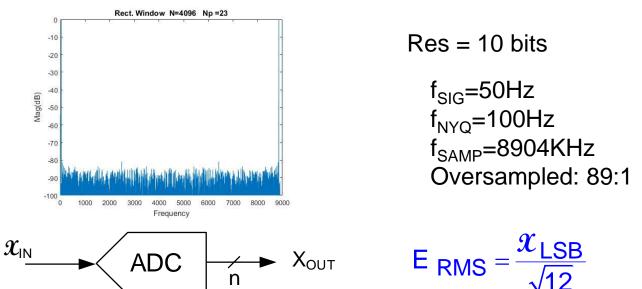


What would happen if we break the 4096 samples into groups of 20 samples and form?

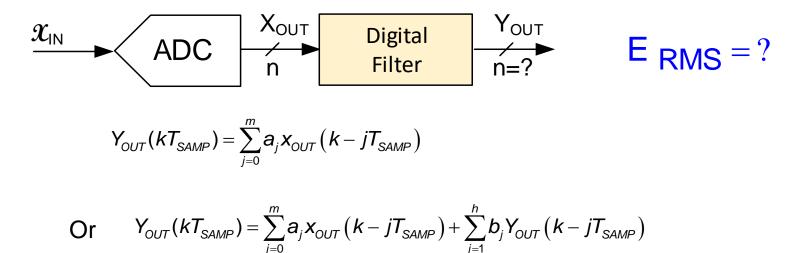
$$\hat{X}_{OUT}(k \bullet 20T_{SAMP}) = \frac{1}{20} \sum_{j=1}^{20} x_{OUT} (jT_{SAMP} + 20kT_{SAMP})$$
 E RMS = ?

- Though the individual samples have been quantized to 10 bits, the arithmetic operations will have many more bits
- The effective sampling rate has been reduced by a factor of 20 but is still over 4 times the Nyquist rate
- Has the quantization noise been reduced (or equivalently has the resolution of the ADC been improved?
- Is there more information available about the signal?

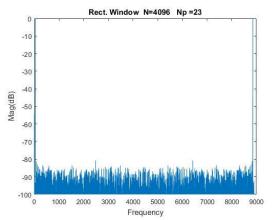




Since the quantization noise is at high frequencies, what would happen if filtered the Boolean output signal?

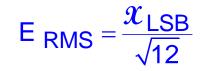






Res = 10 bits

f_{SIG}=50Hz f_{NYQ}=100Hz f_{SAMP}=8904KHz Oversampled: 89:1



What does this difference equation represent?

$$Y_{OUT}(kT_{SAMP}) = \sum_{j=0}^{m} a_j x_{OUT} (k - jT_{SAMP})$$

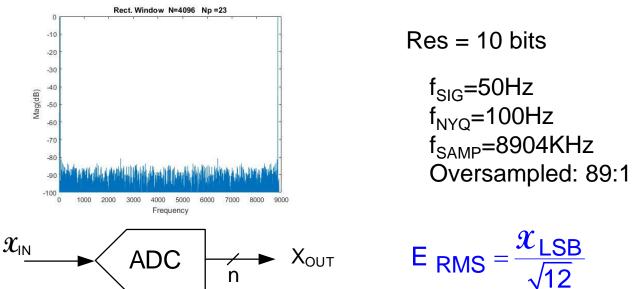
- Moving Average (MA) Digital Filter
- Filter shape (e.g. low-pass, band-pass, high-pass, ... dependent upon <ai> coefficients)

What does this difference equation represent?

$$Y_{OUT}(kT_{SAMP}) = \sum_{j=0}^{m} a_j x_{OUT} \left(k - jT_{SAMP}\right) + \sum_{j=1}^{h} b_j Y_{OUT} \left(k - jT_{SAMP}\right)$$

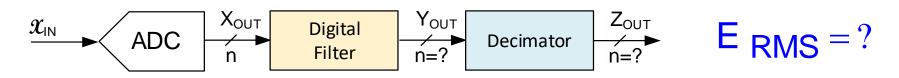
- Auto Regressive Moving Average (ARMA) Digital Filter
- Filter shape (e.g. low-pass, band-pass, high-pass, ... dependent upon <ai> and <bi> coefficients)





Since the quantization noise is at high frequencies, what would happen if filtered and decimated the Boolean output signal?

$$Y_{OUT}(kT_{SAMP}) = \sum_{j=0}^{m} a_j x_{OUT} \left(k - jT_{SAMP} \right)$$
$$Y_{OUT}(kT_{SAMP}) = \sum_{j=0}^{m} a_j x_{OUT} \left(k - jT_{SAMP} \right) + \sum_{j=1}^{h} b_j Y_{OUT} \left(k - jT_{SAMP} \right)$$





Stay Safe and Stay Healthy !

End of Lecture 41